RFIC Solutions Inc.

"Providing Excellence in RF, Analog IC VLSI"

India's leading *VLSI Analog & Mixed Signal, RF IC Design Service* Company...

RFIC Solutions Inc. & Sinhgad Institute Jointly Offer :

Basic Course on VLSI & RF IC Design

Certified Course Contents:

1. About RFIC Solutions Inc.
2. Introduction to Designing of RF IC
3. IC Fabrication process
4. IC Design & IC Layout
5. Hands-on Experience of CAD Tools
6. IC Design Methodologies
7. RF System Level Design
8. Future trends of VLSI
9. Real time IC Design Case Study

Golden opportunity
To become an RF, Analog, Layout IC Professional & Grab a chance to be in Core Semiconductor Industry

Eligibility: *M.Tech, B.Tech, B.E (Elec. /E&T /EE.) B.Sc. (Elect) & Diploma (Elect / E & T/ EE)*
Workshop Venue: *Sinhgad Institute of Technology, Lonawala, Pune.*
Fees: *Rs.4, 000/-Registered before 12th Dec.09 or Rs.5000/- registered after. Lodging and Boarding facility is available at Campus with prior registration in Rs 200/-per Day.*

Duration: *ONE Week*
Date: *21st* **Dec to 25th Dec 2009 (Only 40 seats, Register before 12th Dec. 09)**

Certificate From Semiconductor Industry

Contact Person: Mr. Dilip Chaudhary, 09372810161
Mr.R.V.Babar, 09423558020
Dept. of Electronics & Telecom
Sinhgad Institute of Technology,
Lonawala, Pune.

Contact: **S.M. Technologies Pvt Ltd.**
(Sister Concern, *RFIC Solutions Inc.*)
54 B, "Shree" near BB Tower,
East Shankar nagar,
Nagpur: 440010

Phone: (O) 0712-2522191, 0712-6594060
(M) 09860723739

Website: www.rficsolutions.com
Email: dipchaudhary@rediffmail.com
akorde@rficsolutions.com

At SM Technologies We Build Careers……

Registration:

Registration is limited on first come first served basis.
The course fee per participants is Rs.4,000/-.Each registered participants will be provided course materials & certificates of participation. No TA/DA will be provided. Send your confirmation through mail on *rficsit@gmail.com*. The filled registration form along with DD drawn from any Nationalized Bank in favour of "The Principal, Sinhgad Institute of Technology, Lonavala", Payable at Lonavala. The information will be send before 12th Dec., 2009

Registration Form:

1. Name :
2. Designation :
3. Correspondence Address :

4. Phone No. Off :
5. Mobile No. :
6. Email ID :
7. DD No : Bank :
8. Date : Amount :

9. Place
10. Date:

Address for Correspondence

Department of Electronics & Telecommunication Engg.
Sinhgad Institute of Technology, Lonavala
Pune 410401, MS, India.
02114-304401/355/356/379
Fax No. 91-02114-278304
Email – rficsit@gmail.com

Two Week Basic Training Course @ Sinhgad Institute of Technology, Lonavala

Daily Schedule : 9.30 am to 5.00 pm	7.5 Hours
Morning Session: 9.30 am to1.30 pm	4 Hours
Tea Break: 10.30 am to 10.45 am	15 Minutes
Second Session: 2.00 pm to 5.00 pm	3 Hours
Tea Break: 4.00 pm to 4.15 pm	15 Minutes

EDA Tool will be used in programme:
Agilent's Advanced Design System (ADS)
IC Editor Layout Tool

-	Course Contents	Time
	Day 1	**7.5 Hrs**
1	**Introduction RFIC Solutions Inc.**	**9.30am~11.00am**
	TEA	
2	**Introduction to VLSI**	**11.15am ~ 1pm**
	Impact of Semiconductor Industry, worldwide	
	LUNCH	
3	**Current trends in semiconductor industry**	**2.00pm ~ 3.00pm**
3.1	Introduction RF Semiconductors	**3.00pm ~4.00pm**
	TEA	
4	**IC Fabrication process**	**4.15pm ~ 5.10pm**
	Day 2	**7.5 Hrs**
1.1	CMOS Fabrication Process (Video demo is available)	**9.30am ~ 10.30am**
	TEA	
1.2	RFIC GaAs Fabrication Process	**10.45am ~11.45am**
2	**IC Design Flow**	**11.45am ~ 1.30pm**
	LUNCH	
2.1	Introduction to Full Custom RF IC Design flow and Tool (EDA tool introduction demo)	**2.00pm ~ 4.00pm`**
	TEA	
2.2	IC design process, foundry, PDKs, modern IC design issues	**4.15pm ~ 5.10pm**
2.3	Introduction to layout design and hands on practice with EDA Tool	
	(Schematic, stick dig, Physical design)	
	Day 3	**7.5 Hrs**
1	**Introduction to Different Processes**	**9.30am ~ 1.30pm**
1.1	Introduction to RFCMOS Silicon	
1.2	About SiGe(Silicon Germanium)	
1.3	About GaAs- HBT& pHEMT(Gallium Arsenide)	
1.4	Understanding datasheet specifications	
	LUNCH	
2	**Introdution to Different Simulation**	**2.00pm ~ 3.00pm**
2.1	Different type of Basic Simulation : Simulation Practice Session	**3.00pm ~ 4.00pm**
2.2	Case Study : Design of RF Amplifier with Simulation Practice	**4.15pm ~ 5.00pm**

	Day 4	**7.5 Hrs**
1	**Introduction to RF IC Layout Flow**	**9.30am ~ 1.30pm**
1.1	Introduction to Full Custom RF IC Design layout flow and Tool	
1.2	IC design process, foundry, PDKs, modern IC design issues	
	LUNCH	
2	Practical Session : Layout of RF Amplifier	**2.00pm ~ 4.00pm**
	TEA	
3	Hands on practice with RF IC Layout Tool	**4.15pm ~ 5.00pm**
	Day 5	**7.5 Hrs**
1	**Trade-off of Design**	**9.30am ~ 1.30pm**
1.1	Layout & Design Issues	
1.2	Case Study: Practice Seession	
	LUNCH	
2	Case Study: Practice Session	**2.00pm ~4.00pm**
	TEA	
3	Case Study: Practice Session	**4.15pm ~ 5.00pm**