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Founder President, STES, Pune
Dr. Mrs. S. M. Navale,
Secretary, STES, Pune

Patrons:

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Director, STES-Lonavala Campus &
Principal, SIT, Lonavala.
Dr. A. V. Deshpande,
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Principal, SKNCOE.
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Principal, SCOE, Pune.
Dr. A. G. Kharat
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Dr. P. M. Ghanegaonkar,
Principal, SITS, Narhe,Pune.
Dr. M. G. Bhat
Director (Engineering.), STES, Pune.
Dr. Mrs. J. S. Inamdar
Vice Principal (Admin), SIT, Lonavala.
Dr. K. J. Karande,
Vice Principal(Academic), SIT, Lonavala.

Convener

Dr. D.K. Singh :[+91-9324231055]
Dean R&D, SIT, Lonavala &
HOD, ENTC Dept,
Prof. V.V. Deotare :[+91-9552587386]
ME Coordinator (VLSI & ES)
ENTC Dept.

Coordinators

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Organizing committee:

Prof. D.S. Mantri
Prof. S.B. Gholop
Prof. Mrs.V.M. Rohokale
Prof. Ms. S.S. Patil
Prof. S.M.Kate
Prof. Mrs.V.G.Rajeshwarkar
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Prof. A.A.Labade
Prof. Mrs.S.V. Shinde
Prof. G.G. Vaishnav
Prof.N.A.Lakade
Prof. Ms T.A. Pathade

Registration Fee Particulars:

Research Scholars/PG Students: ₹. 1000/-
Delegates from academic institutions: ₹ 1500/-
ISTE Member: ₹ 1250/-
Delegates from industries: ₹ 2000/-

Accommodation:

External participants will be provided lodging and boarding in college campus at normal rates (₹ 150/per day) provided they should intimate the coordinators about it or must be mentioned in registration form.

REGISTRATION FORM

One Week National Level
Short Term Training Program
ON

"Advanced VLSI and Embedded System"

(November 22nd -26th, 2010)

Name:

Designation:

Correspondence Address:

Mobile No. :

Email ID:
Accommodation needed: Yes/No

DD No. : **Bank**
Date: **Amount:**

Place:

Date:

Signature of Participant:

Signature & seal of Head Of the Institution

Address for Correspondence
Dept. of Electronics & Telecommunication Engg.
Sinhgad Institute of Technology Lonavala,
Pune. 410 401, MS, India.
02114- 304401,304355, 304356, 304379
Fax No: 91-2114 -278304
E-mail: *sit.aves10@gmail.com*

About STES

Sinhgad Technical Education Society (STES) was set up in August 1993, under the able and dynamic leadership of Prof. M.N. Navale with an objective of providing quality education in the field of Dentistry, Engineering, Management, Computer, Pharmacy, Architecture, Hotel Management and the basic school education from kinder garden onwards. There are 58 institutes under the aegis of STES offering full-fledged school education, diploma, Graduation, Post Graduation courses and Ph.D. programs in various branches of Engineering, Science and Management at five educational campuses ideally located in pollution free lush green and picturesque environment conducive for learning. (www.sinhgad.edu)

About SIT

Sinhgad Institute of Technology (SIT), Lonavala since its establishment in 2004 is involved in practicing teaching-learning methodologies of excellence to deliver quality engineering education for students all over India. The institute is housed in a beautiful surroundings, fully residential campus of 160 acres on Pune-Mumbai expressway at Lonavala. Academic discipline with space for individual innovations, emphasis on life skill development of students, 'willing to work' team of faculty members and initiative for Industry Interface, have been the silent activity of the college.

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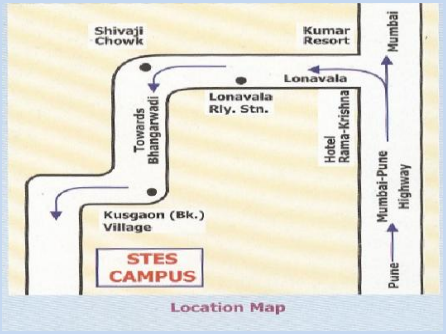
How to reach SIT



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About the STTP:

- This STTP is to provide a platform to understand the recent development in signal processing on FPGA device. It also provides hands on practice to implement different case studies.
- This STTP exposes the faculty to various emerging applications currently in Vogues with expertise scenario. These in turn create interest among faculty in the subject.

STTP program themes

- Signal Processing on FPGA
- Control System on FPGA
- Hands on with ARM Programming
- Real time OS Programming
- Analog CMOS
- Soft CPU Cores in FPGA
- Signal Integrity Issues
- High Speed Digital Design
- Designing with Verilog

Important Dates :

The filled registration form along with DD no. (DD must be drawn from any Nationalized Bank in favor of "The Principal, Sinhgad Institute of Technology, Lonavala", Payable at Lonavala) sent to the address mentioned in registration form, should reach on or before 15th November 2010.

Sponsored by University of Pune

Approved by IETE and ISTE

Sinhgad Institute of Technology Lonavala

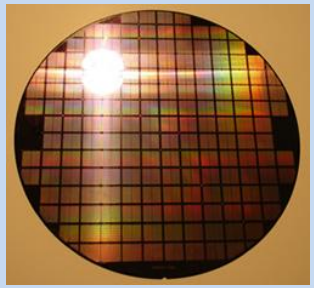
Department of Electronics and Telecommunication Engineering

Organizes

SHORT TERM TRAINING PROGRAM

On

Advanced VLSI & Embedded Systems



(AVES'10)

Nov 22-26, 2010