**IETE Approved**
**National Level**
**Short Term Training Program on**
**"DSP Implementation on FPGA Platform"**
**[STTP: DSP-FPGA]**

**20th June 2012 to 30th June 2012**

## REGISTRATION FORM

(Use photocopy of this form, if needed)

**Name:**_____

**Designation:** _____

**Address:**

_____

_____

**Phone:**_____**FAX:**_____

**Mobile:**_____

**Email:**_____

**Amount: Rs:** _____

**Please find enclosed Demand Draft:**

**No.:**_____**Dated:** _____

Drawn in the favour of

"The Principal, SKNCOE, Pune" payable at "Pune"

**drawn at Bank** _____

**[Cash will also be accepted]**

**Accommodation Required**: YES / NO

Date: Signature

Seal & Signature of Sponsor

## PATRONS:

Hon. Prof. M. N. Navale,
Founder President, STES, Pune
Dr. (Mrs.) Sunanda M. Navale,
Founder Secretary, STES, Pune

## ADVISORY COMMITTEE:

Dr. A. V. Deshpande,
Principal, SKNCOE, Pune.
Dr. K. R. Borole,
Vice Principal, SKNCOE, Pune.
Prof. M. G. Bhat,
Director (Engineering), STES, Pune.
Dr. S. D. Lokhande,
Principal, SCOE, Pune.
Dr. M. S. Gaikwad
Principal, SIT, Lonavala, Pune.
Dr. A. G. Kharat,
Principal, SAE, Kondhava, Pune.
Dr. S. N. Mali,
Principal, SITS, Narhe, Pune.
Dr. S. D. Markande
Director, NBN-SSE, Ambegaon, Pune.
Dr. P. M. Patil
Director, RMD-SSE, Warje, Pune.
Dr. Mrs. Janhavi Inamdar
Principal, SKN-SITS, Lonavala, Pune.

## ORGANIZING COMMITTEE:

Prof. Dr. U. S. Sutar
Prof. S. K. Jagtap
Prof. A. S. Shirsat
Prof. S. S. Agrawal
Prof. S. K. Shah
Prof. M. S. Navale
Prof. R. K. Kulkarni
Prof. A. A. Yadav
Prof. S. S. Vasekar
Prof. V. S. Kulkarni
Prof. K. M. Thakur
Ms. S. M. Borawake
Ms. S. S. Jagdale
Mr. J. B. Amber
Mr. P. S. Kokare

Prof. A. D. Kumbhar
Prof. S. M. Ingawale
Prof. S. M. Koli
Prof. M. M. Dewasthale
Prof. S. K. Sahasrabudhe
Prof. S. A. Panwar
Prof. A. Y. Deshpande
Prof. S. A. Taywade
Prof. S. M. Mali
Prof. R. G. Kulkarni
Prof. P. S. Ingole
Ms. S. U Sadekar
Ms. R. M. Jagtap
Mr. S. M. Kole
Mr. M. M. Damakale

Neha Creations (020) 24252131

IETE
The Institution of Electronics and Telecommunication Engineers

# IETE Approved
## National Level
## Two weeks
## Short Term Training Program
## on
# "DSP Implementation on FPGA Platform"
## [STTP: DSP-FPGA]
## 20th to 30th June 2012

**Organized by**

Department of Electronics and
Telecommunication Engineering,
STES's
**Smt. Kashibai Navale College of Engineering,**
Pune - 411 041. Maharashtra.
Tel: 020-24100295 Fax: 020-24354938

www.sinhgad.edu
E-mail : sttpvlsidsp@gmail.com

**Convener**

Prof. Dr. P. Mukherji, HOD (E&TC)

**Co-ordinator**

Prof. Mrs. P. S. Deshpande (M: 7350338133)
Prof. Mrs. R. H. Jagdale (M: 9923184950)
Prof. Mr. H. S. Thakar (M: 9881740472)
Prof. Mr. P. G. Chilveri (M: 9881739074)

## About STES

Sinhgad Technical Education Society (STES) was set up in August 1993 under the able and dynamic leadership of Hon. Prof. M. N. Navale with an objective of providing quality education in the field of Dentistry, Engineering, Management, Computer, Pharmacy, Medical Education, Physiotherapy, Nursing, Architecture, Hotel Management and basic school education from Kinder Garden onwards. There are 100 institutes under the aegis of STES offering full-fledged school education, Diploma, Graduation, Post Graduation courses and Ph.D. programs in various branches of Engineering, Science and Management at seven educational campuses, ideally located in pollution free lush green picturesque environment conducive for learning.

## About SKNCOE

Smt. Kashibai Navale College of Engineering (SKNCOE), established in the year 2001 is one of the foremost colleges under University of Pune. It is approved by the All India Council for Technical Education (AICTE), New Delhi & affiliated to University of Pune. SKNCOE has been accredited by National Board of Accreditation (N.B.A.), New Delhi.

SKNCOE offers Full Time, Bachelor of Engineering (B.E.) Programs of University of Pune in Electronics & Telecommunication Engineering, Computer Engineering, Information Technology and Mechanical Engineering. It also offers full time Masters programme in Business Administration (MBA) and Engineering (ME-Signal Processing, VLSI and Embedded Systems, Computer Sciences).

The college has well-qualified, devoted and dedicated team of teaching staff members. Quality Technical Education is provided to the students in order to meet challenges of Globalization with state of the art equipment and laboratories. The college has consistently excelled in academics and extracurricular activities.

## WHO CAN ATTEND?

The academicians, students and researchers with Electronics / Telecommunication, Computer Science, Information Technology background, who are working or intending to work in the areas of Digital Signal Processing and VLSI Design, will be most benefited by this course.

## PURPOSE OF COURSE:

The purpose of the STTP: DSP-FPGA is to explore latest technological trends in implementation of DSP based applications on FPGA Platform, which will be helpful to academicians for enhancing their knowledge about subject contents like Digital Signal Processing and VLSI Design working at UG/PG Level. The activity is planned to facilitate the participants to experience and experiment the knowledge for academic and research work in an effective manner. It is an inter-institutional activity for utilizing the expertise from various institutes and industries. The course will consist of brain storming sessions and laboratory work by experts from Industries, R&D centers and top class institutions. .

## TOPICS (Tentative but not limited):

- **Fundamentals and Advances in Signal Processing.**
- **Design Tools and Techniques of DSP-FPGA platform.**
- **Fundamental and Advances in Image Processing.**
- **Wavelets and its Applications**
- **Video Processing**
- **Automatic Speech Recognition using Statistical Approach**
- **Speaker Verification**
- **Implementation of Audio, Video and Speech Processing on FPGA.**
- **Emerging Technologies: VLSI/DSP**

## SPEAKERS:

**Eminent personalities from various organizations like IIT Bombay, C-DAC Pune, TIFR Mumbai, SGGS Nanded, COEP Pune, SKNCOE Pune and CoreEL Technologies Pune will be the resource persons.**

## ACCOMMODATION:

Request for the accommodation is to be made along with the submission of registration form preferably two days in advance. Please note that accommodation will be provided in campus.
Contact Person- Mr. P. S. Kokare - 09850539362

## REGISTRATION:

- The course fee- Rs. 5,000/- for faculty from Academic Institution, Rs. 4,000/- for PG/UG students and Rs. 6,000/- for others.
- Each registered participants will be provided course materials, working, lunch, tea and certificate of participation.
- Last date for registration is 1st June. 2012.
- The filled registration form along with the Demand Draft drawn from any Nationalized Bank in the favour of "The Principal, SKNCOE, Pune" payable at "Pune" required to be sent to the address given below:

**Prof. Ms. R. H. Jagdale**
**Coordinator, STTP: DSP-FPGA,**
**Dept. of E&TC Engineering**
**Smt. Kashibai Navale College of Engineering,**
**S.No:44/1, Vadgaon (Bk.),**
**Off Sinhgad Road, Pune - 411 041, Maharashtra.**
**Mob: 09923184950.**